REMARKS

Claims 1-8 are pending in this application, of which claims 1 and 2 have been amended. No new claims have been added.

In the FINAL Office Action mailed December 20, 2005, the Examiner has requested a new, more descriptive title.

Accordingly, the title has been amended to read: A Method Of Manufacturing A Packaging Structure For Electronic Parts Buried In An Insulating Film Formed On The Electronic Parts And A Wiring Substrate.

In the FINAL Office Action mailed December 20, 2005, the Examiner rejected claims 1-3 under 35 U.S.C. § 102(e) as anticipated by **Umetsu et al.** (previously applied).

Applicants respectfully traverse this rejection.

As noted in Applicants' previous response filed December 5, 2005, **Umetsu et al.** discloses a method of forming a semiconductor device in which a conductive material is provided to an open end of a penetrating hole 24 penetrating through the semiconductor element, on the side of a first surface of the semiconductor element. The conductive material is melted to flow into the penetrating hole. The conductive material is made to flow into the penetrating hole in a state that an atmospheric pressure on the side of a second surface of the semiconductor element opposite to the first surface is lower than an atmospheric pressure on the side of the first surface.

FIG. 2A shows that penetrating hole 24 is formed in an insulating material 22 covering one side of the semiconductor chip, and extends through the semiconductor chip 10 and the conductive pad 14 (and metal covering 16). Conductive material 40 is forced through the penetrating hole 24 so as to provide a rounded conductive surface on opposite sides of the semiconductor device.

The Examiner urges that items 14, 16 correspond to the wiring patterns of the instant application as shown, for example, in FIG. 1H as wiring pattern 32a.

Applicants respectfully disagree. Items 14, 16 in **Umetsu et al.** are merely conductive pads formed on the semiconductor chip 10, and metal layers provided on the pads to prevent oxidation of the pads, respectively, and are not formed on the insulating film in which the semiconductor chip is buried, as in the present invention. **Umetsu et al.** is directed to forming a semiconductor device, and not to a method of making packaging structure for the semiconductor device, to which the claims of the instant application are directed. Item 1 of **Umetsu et al.** is a single semiconductor device including a single semiconductor chip 10. FIG. 4 shows several of the semiconductor devices 1 stacked on top of each other, but does not show the steps of manufacturing an electronic parts packaging structure, as recited in claims 1-3 and 5-7, where the "electronic parts" (corresponding to the semiconductor device 1 of **Umetsu et al.**) are covered by an insulating form, and a via hole is formed in the insulating film to reach the connection terminal of the "electronic parts" (semiconductor device), as recited in claims 1 and 2 of the instant application.

Furthermore, in the FINAL Office Action, the Examiner urged:

> In regards to the argument that items 14 & 16 are "merely conductive pads and metal layers provided on the pads to prevent oxidation of the pads," the examiner directs the applicant to Umetsu et al., lines 2-3 of paragraph [116], "Each pad 14 is an electrode of an integrated circuit formed in the semiconductor chip 10." Lines 13-15 of paragraph [116] also state, "Note that a passivation film (not shown) may further be formed on the surface of the semiconductor chip 10 on which the pads 14 are formed."
>
> Therefore, there is an integrated circuit/wiring pattern formed on and/or in chip 10 and optionally covered by a passive/"insulating" layer (not shown in drawings) on one side and insulating film 22 on the other side. The package structure can be then mounted on a wiring substrate 80, as shown in figure 10. (Sic.)

Applicants respectfully disagree with the Examiner on two points.

First, an "electrode of an integrated circuit" in **Umetsu et al.** is not the same as the "wiring pattern" recited in claim 1 of the instant application.

Second, claim 1 of the instant application recites that the "overlying wiring pattern" is formed on the insulating film. In contrast, **Umetsu et al.** discloses only that the passivation film is formed on the surface of the semiconductor chip 10, and that pads 14 are formed on the semiconductor chip 10. There is no disclosure in **Umetsu et al.** that the pads 14 are formed on the passivation film.

The Examiner further urges that the overlying wiring pattern formed on the insulating layer in claim 1 of the instant application also corresponds to pad 14 and metal layer 16 in FIG. 3 of **Umetsu et al.** Pad 14 and metal layer 16 of **Umetsu et al.** are formed on a surface opposed to the surface that insulating material 22 of semiconductor chip 20 is formed. Accordingly, claim 1

of the instant application and **Umetsu et al.** are completely different. In claim 1 of the instant application, the wiring pattern on the base substrate and the overlying pattern formed on the insulating film on the electronic parts cannot be equal.

Also, in **Umetsu et al.**, the insulating material 22 is only formed on the upper surface of semiconductor chip 10, and the insulating material 22 does not bury the entire semiconductor chip 20. Only lamination of a plurality of the semiconductor chips 10 is described, and the semiconductor chip is not mounted on the wiring substrate.

In the FINAL Office Action mailed December 20, 2005, the Examiner rejected claim 4 under 35 U.S.C. § 103(a) as unpatentable over **Umetsu et al.** in view of U.S. Patent 6,363,513 to Furukawa et al. (hereafter, "**Furukawa et al.**").

Applicants respectfully traverse this rejection.

Furukawa et al. discloses a method of manufacturing a semiconductor device in which a via hole having a bottom is formed in a substrate and then a conductor layer is formed at least over a sidewall of the via hole. Thereafter, the substrate is thinned by removing a portion of the substrate opposite another portion of the substrate in which the via hole is formed such that the conductor layer is exposed.

Furukawa et al. has been cited for teaching the use of an electroplating method to form a connection terminal but, like **Umetsu et al.** discussed above, is not directed to a method of manufacturing an electronic parts packaging structure in which the electronic parts are flip-chip connected to a wiring substrate such that the electronic parts are buried in an insulating film, as in the present invention.

In the FINAL Office Action, the Examiner rejected claim 8 under 35 U.S.C. § 103(a) as unpatentable over **Umetsu et al.**

Applicants respectfully traverse this rejection.

The Examiner has indicated that no criticality has been shown regarding the recited limitation of 150 micrometers or less for the thickness of the semiconductor chip.

As noted above, **Umetsu et al.** is not directed to a method of manufacturing an electronic parts packaging structure, as recited in claim 1, from which claim 8 depends.

In view of the aforementioned amendments, claims 1-8, as amended, are in condition for further examination.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

William L. Brooks
Attorney for Applicant
Reg. No. 34,129

WLB/ak
Atty. Docket No. **031287A**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosures: Request for Continued Examination Transmittal
Check in the amount of $790.00

Q:\HOME\AKERR\WLB\03\031287a\preliminary amendment feb 2006